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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/921,741	08/01/2001	Michael Tate	41257/PAN/X2/134038	8731

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EXAMINER	
CHEN, ALAN S	

ART UNIT	PAPER NUMBER
2182	6

DATE MAILED: 02/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/921,741	TATE, MICHAEL	
	Examiner	Art Unit	
	Alan S Chen	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 November 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28 and 46-50* is/are pending in the application.

4a) Of the above claim(s) *29-45* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28 and 46-50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08/01/01* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Election/Restrictions

1. Applicant's election of claims 1-28 and 46-50 in Paper No. 4 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: elements 506 and 508 of Fig. 6. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 18 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5. Applicant cites the first width being 68, but this is not indicated anywhere in the specification. Examiner assumes first width is 32 bits in his Office Action.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1, 8-10, 13, 17-23, 26-28, 46-48 and 50 are rejected under 35 U.S.C. 102(b) as being anticipated by No. US005950223A to Chiang et al. (hereafter Chiang).

8. As per claim 1, Chiang discloses a method for maintaining throughput in a data element (Fig. 3, maintaining throughput at both clock edges, the data element being a DRAM), comprising the steps of: receiving a clock (Fig. 5A and 5B CAS clock lines) and a plurality of instances of data having a first width (Fig. 7A, element DQ) on an input; processing (e.g., latching 32-bit data, Column 3, lines 52-58) consecutive ones of the plurality of instances of data having the first width (32-bit data latched, and upon the next clock edge, producing another 32-bit data to be latched) to produce more than one of a plurality of instances of data having a second width wherein the second data width are equivalent to the first data width (Fig. 7A, DO1, DO2 and DOn are all the same width, and the first width is picked up on the rising edge of CAS, while the second width is picked up on the falling edge of the clock, hence dual data/edge rate sampling of data) and the more than one of the plurality of instances of data having the second data width are used to produce a plurality of instances of data having a third data width (Column 3, lines 52-58, 64-bit data produced with both first and second width data) wherein the third data width are greater than the second data width the plurality of instances of data having a third data width are used to produce a plurality of instances of data having an output data width (output of 64-bit data may be placed into an I/O buffer for instance, Fig. 3, element 334) wherein the output data width are equivalent to the third data width (I/O buffer is same 64-bit width as the 64-bit latch that was produced from two 32-bit words); and transmitting the plurality of instances of

data having the output data width and transmitting the plurality of instances of data having the third data width (transmission out of memory device Fig. 3 via a read operation).

9. As per claim 8-10, Chiang discloses the method of claim 1, where the processing step includes sampling the data at dual clock edges at the rising and falling edge of a clock (Fig. 7A) each sample being 32 bits (first and second width) and the producing a 64 bit word (third and fourth width (Column 3, lines 50-58)).

10. As per claim 13, Chiang discloses the method of claim 1 wherein the processing step comprises the step of resolving a data alignment (the use of 64 bit data is aligned using two 32 bit data obtained from consecutive rising and falling clock edges, Fig. 7A).

11. As per claim 17, Chiang discloses a method for maintaining throughput in a data element (Fig. 3), comprising the steps of: receiving at a first element a clock (Fig. 5, CAS) and a first plurality of instances of data having a first bit-width as an input (Fig. 5, Data, fixed width); transmitting the clock and first plurality of instances of data having the first width (Data associated with 1st strobe) to a second element; operating on the first plurality of instances of data having the first width to produce a second plurality of instances of data having a second width (data associated with 2nd strobe); transmitting the clock and second plurality of instance of data having the second width to a third element (Memory array in Fig. 3 can be the third element); operating on the second plurality of instances of data having the second width to produce a third plurality of instances of data having a third width (Column 3, lines 50-58); transmitting the third plurality of instances of data having the third width to a fourth element (I/O buffers); and operating on the third plurality of instances of data having the third width to produce a fourth plurality of instances of data having a fourth width (width of each buffer line, in

Fig. 3, this shows a 32 (3rd width) to 16 (4th width) bit conversion, but can be different as indicated in Column 3).

12. As per claims 18 and 19, Chiang discloses the method according to claim 17, wherein the first and second width is 32 (Column 3, lines 50-58).

13. As per claims 20-22, Chiang discloses the method according to claim 17, wherein the third and fourth width is 64 (Column 3, lines 50-58).

14. As per claim 23, Chiang discloses the method according to claim 17, further comprising the steps of: receiving the fourth plurality of instances of data having the fourth width by a fifth element (Fig. 3, the memory array is the third element, the column decoder is the fourth element and the I/O buffers is the fifth element); and transmitting a fifth plurality of instances (16 bits) of data having a fifth width which is half of the fourth width (32 bits).

15. As per claims 26-28, Chiang discloses the method according to claim 17, wherein the third element is a receive function element (Fig. 3, element 326 is the memory array, receiving data to be written to it), the fourth element is a receive control element (decoder controls what gets output from what it receives from the memory array), and the fifth element is a system interface (I/O buffer to another device).

16. As per claim 46, Chiang discloses a method for maintaining throughput in a data element (Fig. 3), comprising the steps of: receiving a first data having first bit-width bits (Fig. 3, element 334), management bits and clock bits (Fig. 3, signals lines OE, WE, CASH, CASL, etc); inputting the first bit-width bits and clock bits into a receive path (receive data paths show as lines to modules); and processing the first bit-width bits to generate processed data having a

second bit-width which is greater than said first bit width (Column 3, line 50-58, where 32 bits is the first width while 64 bits is the second width).

17. As per claims 47 and 48, Chiang discloses the method of claim 46, wherein the processing step further comprises: receiving a clock having a clock rate (Fig. 7A, CAS line has periodicity which equals a rate); and performing dual data rate sampling (rising and falling edge sampling of the clock, Fig. 7A) on the first bit width data in accordance with said clock to produce the processed data having a second bit-width which is greater than the first bit-width (Column 3, lines 50-58, where 32 bits is first width, 64 bits is second width).

18. As per claim 50, Chiang discloses the method of claim 47, wherein the step of performing dual data rate sampling on the first bit-width bits comprises inputting the first bit-width bits to two gates (Fig. 5A strobe signals 1 and 2 are gates that latch data at rising and falling edge of clock CAS), one gate triggering at a rising edge of the clock (Fig. 5A, 1st data strobe) and the other gate triggering on a falling edge of the clock (Fig. 5A, 2nd data strobe).

Claim Rejections - 35 USC § 103

19. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

20. Claims 2-4, 15 and 16 are rejected under 35 USC 103(a) as being unpatentable over Chiang in view of PCI Local Bus Specification Rev. 2.1 (hereafter PCI Spec).

21. As per claim 2-4 and 15 Chiang discloses the method according to claim 1, the processing step further comprising the steps of sampling consecutive ones of the plurality of

instances (Fig. 7A) having the first width at consecutive ones of a first rising edge and falling edge of the clock (DO1 and DO2 of 7A can be the first width); generating more than one instance of a plurality of data having the second width (the second width is the same as the first width); Chiang further discloses generating and transmitting a third width that is double the first and second width (Column 3, lines 50-58).

Chiang does not expressly disclose converting the more than one instance of the plurality of data having the second width at a second rising edge of the clock to result in the plurality of instances of data having the third width data or transmitting a handshake signal; and transmitting the plurality of instances of data having the third data width.

PCI Spec discloses ability for the PCI bus to handle 64 bit data and addressing. PCI Spec details what is needed in latching in an additional 32 bits of data and the handshaking required (e.g., ACK64 and REQ64, page 16 of PCI Spec which are pulses, specifically sustained pulses, page 8, s/t/s). Furthermore, PCI Spec uses the rising edge of the clock, and hence, the second 32-bit piece of data is latched in on the second rising edge after the first one is latched in.

Chiang and PCI Spec are analogous art because they are from the same field of endeavor in how to increase throughput on a data bus.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to used handshaking and latch data on the second rising edge of the clock.

The suggestion/motivation for doing so would have been the need to request/acknowledge a double word bit transfer in a bussing/addressing system that transfers only one word per clock edge. Furthermore, this follows an omnipresent bus specification used and well known to the entire computer industry.

Therefore, it would have been obvious to combine Chiang with PCI Spec for the benefit of transferring a double word on single word bus architecture and abiding by a well-established specification.

22. As per claim 16, Chiang combined with PCI Spec discloses the method according to claim 15, wherein Chiang further specifies the use of I/O buffers (encompassing FIFOs) to be used in I/O transactions (Fig. 3, element 334), where handshaking could occur.

23. Claims 5 and 49 rejected under 35 USC 103(a) as being unpatentable over Chiang in view of PCI Spec.

Chiang combined with PCI Spec and Chiang discloses claims 1 and 41, respectively. Chiang and PCI Spec do not disclose expressly the clock being received from a media independent interface.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to receive the clock from a media independent interface.

The suggestion/motivation for doing so would have been the generic memory implementation described by Chiang can be used wherever there requires a storage location, and a media independent interface is no exception. Further PCI Spec is also a generic specification. Both show the clock coming in from an external source.

Therefore, it would have been obvious receive the clock from an external source such as a media independent interface for the benefit of the generic memory receiving a clock signal from the outside since it is not generated internally.

24. Claims 6, 7, 11, 12, 14, 24, 25 rejected under 35 USC 103(a) as being unpatentable over Chiang in view of No. US005812792A to Haddock et al. (hereafter Haddock).

Chiang discloses claims 1 and 17.

Chiang does not disclose expressly his generic DRAM implementation used in a network system, and therefore not having CRC, statistics generation, resolving inter-packet gap, resolving preamble detection, resolving statistics, having a physical layer device, or a management control element.

Haddock discloses using DRAM in a network system, having CRC (Column 8, lines 48-67), statistics generation (Column 16, lines 40-65), resolving inter-packet gap (timing differences resolution, Column 16, lines 32-39), resolving preamble detection (Fig. 11, preamble in frame), resolving statistics (Column 16, lines 40-65), having a physical layer device (Fig. 2), or a management control element (Fig. 5).

Chiang and Haddock are analogous art because they are from the same field of endeavor in the use and implementation of DRAM.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Chiang's DRAM in a network system.

The suggestion/motivation for doing so would have been to be able to accommodate multiple clients who have multiple displays requiring video DRAM) on a network (Fig. 1), and hence requiring fast memory access that Chiang provides with sampling on the rising and falling edges of the clock.

Therefore, it would have been obvious to combine Chiang with Haddock for the benefit of fast video DRAM in a network environment.

Conclusion

25. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to further show the state of the art with respect to adjusting sampling at rising and falling edges applicable to networks:

U.S. Pat. No. 4,984,195 to Nakamura et al.

U.S. Pat. No. US005142556A to Ito

U.S. Pat. No. US005159679A to Culley

U.S. Pat. No. US005341488A to Kobayashi

U.S. Pat. No. US005754875A to Getzlaff et al.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alan S Chen whose telephone number is 703-605-0708. The examiner can normally be reached on M-F 8:30am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey A Gaffin can be reached on 703-308-3301. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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